AMENDMENTS TO THE CLAIMS

19. (previously presented) A process for preparing a single crystal silicon wafer, the process comprising thermally annealing a single crystal silicon wafer at a temperature in excess of about 1000°C in an atmosphere of hydrogen, argon, oxygen, nitrogen, or a mixture thereof, said wafer having a central axis, a front side and a back side which are generally perpendicular to the central axis, a central plane between the front and back sides, a circumferential edge, a radius extending from the central axis to the circumferential edge, a first axially symmetric region extending radially inward from the circumferential edge in which silicon self-interstitials are the predominant intrinsic point defect and which is substantially free of agglomerated interstitial defects, a second axially symmetric region, located radially inward of the first axially symmetric region, in which vacancies are the predominant intrinsic point defect and which is substantially free of agglomerated vacancy defects, and a third axially symmetric region, located radially inward of the second axially symmetric region, which comprises agglomerated vacancy defects, the thermal anneal acting to dissolve agglomerated vacancy defects present in the third axially symmetric region within a layer extending from the front side toward the central plane.

20. (original) The process as set forth in claim 19 wherein the wafer is thermally annealed in an argon atmosphere.

21. (original) The process as set forth in claim 19 wherein the wafer is thermally annealed by heating the wafer to a temperature ranging from about 1100 to about 1300°C.

22. (original) The process as set forth in claim 21 wherein the wafer is thermally annealed for about 1 to about 4 hours.

23. (original) The process as set forth in claim 19 wherein the wafer is thermally annealed by heating the wafer to a temperature ranging from about 1200 to about 1250°C.

24. (original) The process as set forth in claim 23 wherein the wafer is thermally annealed for about 2 to about 3 hours.

25. (original) The process as set forth in claim 19 wherein the layer extends from the front side and toward the central plane to a depth of about 4 microns.

26. (original) The process as set forth in claim 19 wherein the layer extends from the front side and towards the central plane to a depth of about 8 microns.

27. (original) The process as set forth in claim 19 wherein the layer extends from the front side and towards the central plane to a depth of about 10 microns.

28. (original) The process as set forth in claim 19 wherein the layer extends from the front side and towards the central plane to a depth of about 20 microns.

29. (original) The process as set forth in claim 19 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 10% the length of the radius.

30. (original) The process as set forth in claim 19 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 30% the length of the radius.

31. (original) The process as set forth in claim 19 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 60% the length of the radius.

32. (original) The process as set forth in claim 19 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 80% the length of the radius.

33. (original) The process as set forth in claim 19 wherein the wafer has a diameter of at least about 150 mm.

34. (original) The process as set forth in claim 19 wherein the wafer has a diameter of at least about 200 mm.

35. (currently amended) A process for preparing a silicon wafer having a surface layer which is substantially free of agglomerated intrinsic point defects, the wafer being sliced from a single crystal silicon ingot having a central axis, a seed-cone, an end-cone, and a constant diameter portion which extends between the seed-cone and the end-cone, the constant diameter portion having a circumferential edge and a radius extending from the circumferential edge toward the central axis, the ingot being grown from a silicon melt and then cooled from the solidification temperature in accordance with the Czochralski method, the process comprising:

growing the single crystal silicon ingot, wherein the growth velocity, v, and an average axial temperature gradient, G_0, are controlled during the growth of the constant diameter portion of the ingot over a temperature range from solidification to a temperature of no less than about 1325 °C to cause the formation of a segment of the constant diameter portion which, upon cooling of the ingot from the solidification temperature, comprises a first axially symmetrical region extending radially inward from the circumferential edge toward the central axis in which silicon self-interstitials are the predominant intrinsic point defect and which is substantially free of agglomerated interstitial defects, and a second axially symmetric region in which vacancies are the predominant intrinsic point defect, wherein, as part of the cooling process, the ingot is cooled through a temperature range from the solidification temperature of silicon to about 800 °C at a cooling rate which ranges from about 0.1 to about 1.5 °C/min;

slicing the segment of the constant diameter portion to obtain a wafer, the wafer having a front side and a back side which are generally perpendicular to the central axis, and a central plane between the front and back sides, the wafer comprising the first and second axially symmetric regions; and,

thermally annealing the wafer at a temperature in excess of about 1000°C in an atmosphere of hydrogen, argon, oxygen, nitrogen, or a mixture thereof to dissolve agglomerated vacancy defects present in the second axially symmetric region within a layer extending from the front surface toward the central plane of the wafer such that the layer is substantially free of agglomerated intrinsic point defects.

36. (original) The process as set forth in claim 35 wherein the wafer is thermally annealed in an argon atmosphere.

37. (original) The process as set forth in claim 35 wherein the wafer is thermally annealed by heating the wafer to a temperature ranging from about 1100 to about 1300°C.

38. (original) The process as set forth in claim 37 wherein the wafer is thermally annealed for about 1 to about 4 hours.

39. (original) The process as set forth in claim 35 wherein the layer extends from the front side and toward the central plane to a depth of at least about 4 microns.

40. (original) The process as set forth in claim 35 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 60% the length of the radius.

41. (previously presented) The process as set forth in claim 19 wherein the wafer is sliced from a single crystal silicon ingot grown and cooled in accordance with the Czochralski method, such that as part of the cooling process the ingot is cooled at a cooling rate which ranges from about 0.1 to about 3.0 °C/min.

42. (previously presented) The process as set forth in claim 41 wherein as part of the cooling process the ingot is cooled through a temperature rate from the solidification temperature of silicon to about 800 °C at a cooling rate which ranges from about 0.1 to about 3.0 °C/min.

43. (previously presented) The process as set forth in claim 42 wherein the cooling rate ranges from about 0.1 to about 1.5 °C/min.

44. (previously presented) The process as set forth in claim 42 wherein the cooling rate ranges from about 0.1 to about 1.0 °C/min.

45. (previously presented) The process as set forth in claim 42 wherein the cooling rate ranges from about 0.1 to about 0.5 °C/min.

46. (previously presented) The process as set forth in claim 19 wherein the wafer has a diameter of at least about 300 mm.

47. (previously presented) The process as set forth in claim 19 wherein the second axially symmetric region has a width of at least about 7.5% of the radius of the wafer.

48. (previously presented) The process as set forth in claim 19 wherein the second axially symmetric region has a width of at least about 15% of the radius of the wafer.

49. (previously presented) The process as set forth in claim 19 wherein the second axially symmetric region has a width of at least about 25% of the radius of the wafer.

50. (previously presented) The process as set forth in claim 19 wherein the second axially symmetric region has a width of at least about 50% of the radius of the wafer.

51. (cancelled)

52. (cancelled)

53. (cancelled)

54. (currently amended) The process as set forth in claim ~~52~~ 35 wherein the cooling rate ranges from about 0.1 to about 1.0 °C/min.

55. (currently amended) The process as set forth in claim ~~52~~ 35 wherein the cooling rate ranges from about 0.1 to about 0.5 °C/min.

56. (previously presented) The process as set forth in claim 35 wherein the wafer has a diameter of at least about 300 mm.

57. (currently amended) A process for preparing a single crystal silicon wafer having a surface layer which is substantially free of agglomerated intrinsic point defects, the process comprising thermally annealing a single crystal silicon wafer at a temperature in excess of about 1000°C in an atmosphere of hydrogen, argon, oxygen, nitrogen, or a mixture thereof, said wafer having been sliced from a single crystal silicon ingot grown and cooled in accordance with the Czochralski method wherein, as part of the cooling process, the ingot was cooled through a temperature range from the solidification temperature of silicon to about 800 °C at a cooling rate which ranges from about 0.1 to about 1.5 °C/min, and said wafer having a central axis, a front side and a back side which are generally perpendicular to the central axis, a central plane between the front and back sides, a circumferential edge, a radius extending from the central axis to the circumferential edge, a first axially symmetric region extending radially inward from the circumferential edge in which silicon self-interstitials are the predominant intrinsic point defect and which is substantially free of agglomerated

interstitial defects, and a second axially symmetric region, located radially inward of the first axially symmetric region, in which vacancies are the predominant intrinsic point defect, the thermal anneal acting to dissolve agglomerated vacancy defects present in the second axially symmetric region within a layer extending from the front side toward the central plane such that the layer is substantially free of agglomerated intrinsic point defects.

58. (previously presented) The process as set forth in claim 57 wherein the wafer is thermally annealed in an argon atmosphere.

59. (previously presented) The process as set forth in claim 57 wherein the wafer is thermally annealed by heating the wafer to a temperature ranging from about 1100 to about 1300°C.

60. (previously presented) The process as set forth in claim 59 wherein the wafer is thermally annealed for about 1 to about 4 hours.

61. (previously presented) The process as set forth in claim 57 wherein the wafer is thermally annealed by heating the wafer to a temperature ranging from about 1200 to about 1250°C.

62. (previously presented) The process as set forth in claim 61 wherein the wafer is thermally annealed for about 2 to about 3 hours.

63. (previously presented) The process as set forth in claim 57 wherein the layer extends from the front side and toward the central plane to a depth of about 4 microns.

64. (previously presented) The process as set forth in claim 57 wherein the layer extends from the front side and towards the central plane to a depth of about 8 microns.

65. (previously presented) The process as set forth in claim 57 wherein the layer extends from the front side and towards the central plane to a depth of about 10 microns.

66. (previously presented) The process as set forth in claim 57 wherein the layer extends from the front side and towards the central plane to a depth of about 20 microns.

67. (previously presented) The process as set forth in claim 57 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 10% the length of the radius.

68. (previously presented) The process as set forth in claim 57 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 30% the length of the radius.

69. (previously presented) The process as set forth in claim 57 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 60% the length of the radius.

70. (previously presented) The process as set forth in claim 57 wherein the first axially symmetric region has a width, as measured from the circumferential edge radially toward the center axis, which is at least about 80% the length of the radius.

71. (previously presented) The process as set forth in claim 57 wherein the wafer has a diameter of at least about 150 mm.

72. (previously presented) The process as set forth in claim 57 wherein the wafer has a diameter of at least about 200 mm.

73. (previously presented) The process as set forth in claim 57 wherein the wafer has a diameter of at least about 300 mm.

74. (cancelled)

75. (cancelled)

76. (cancelled)

77. (currently amended) The process as set forth in claim ~~75~~ 57 wherein the cooling rate ranges from about 0.1 to about 1.0 °C/min.

78. (previously presented) The process as set forth in claim ~~75~~ 57 wherein the cooling rate ranges from about 0.1 to about 0.5 °C/min.